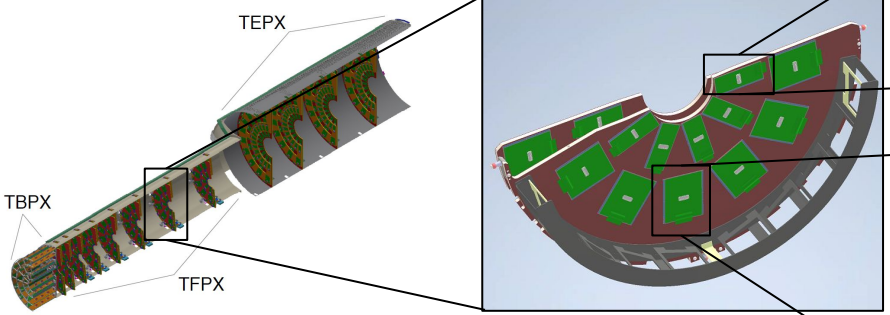
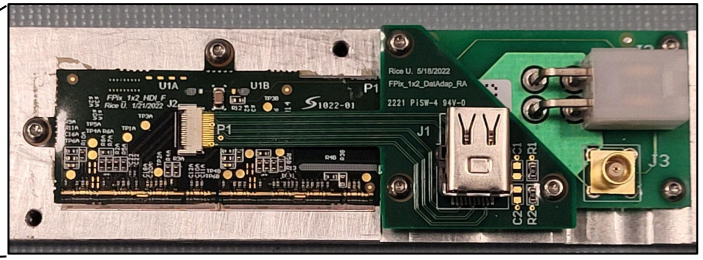
Pixel Module Testing

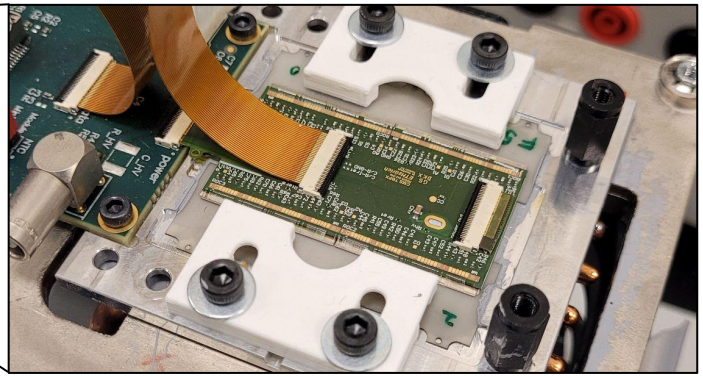


Inner Tracker

Dee Cartridge

Prototype 2x1 Module



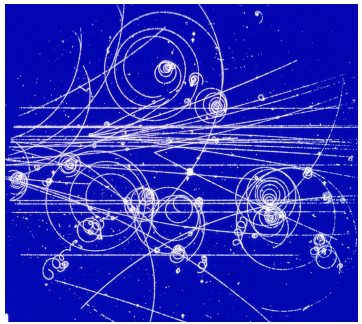


Prototype 2x2 Module

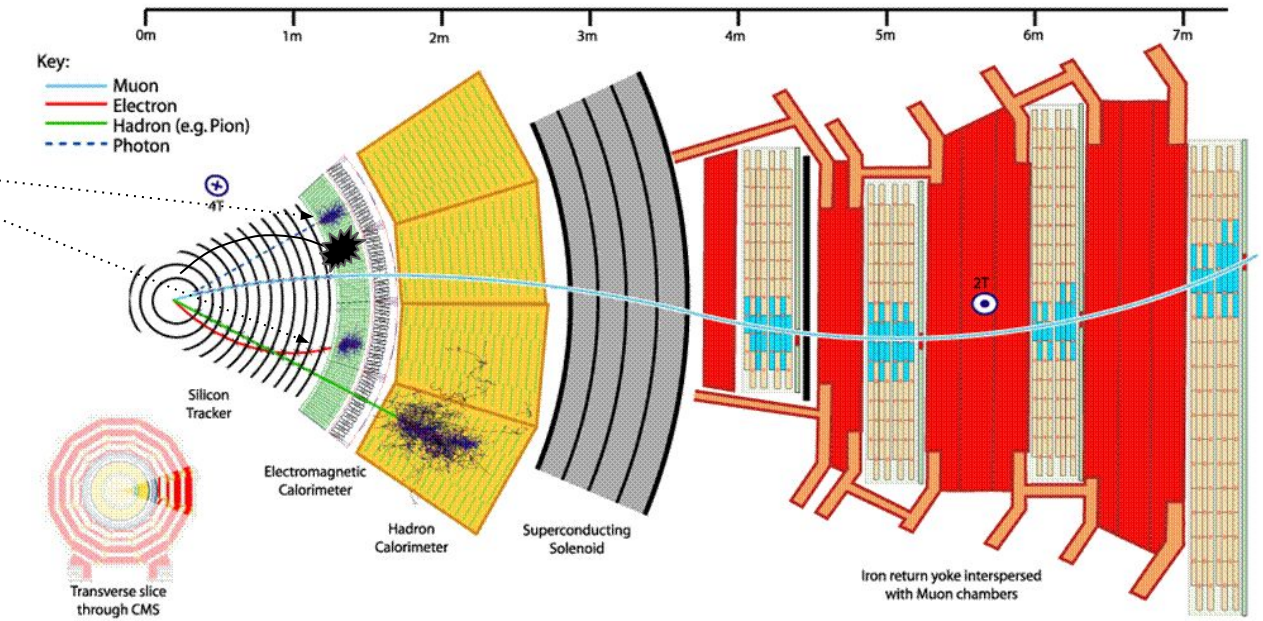
A Tracker? Why?

A brief reminder:

- Particle identification γ vs e
- Momentum
- Displaced vertices



The decay of a lambda particle in the 32cm hydrogen bubble chamber



CMS particle detection summary

What do we need (HL-LHC)

Temporal and Spatial Resolution:

Table 35.1: Typical resolutions and deadtimes of common charged particle detectors. Revised September 2023.

Detector Type	Intrinsinc Spatial Resolution (rms)	Time Resolution	Dead Time
Resistive plate chamber	50 μm	50–1000 ps*	10 ns†
Liquid argon TPC	0.5–1 mm‡	0.01-1 μs§	—¶
Scintillation tracker	∼100 μm	100 ps/n‖	10 ns
Bubble chamber	10–150 μm	1 ms	50 ms**
Wire chambers (proportional and drift chambers)	50–100 μm	5–10 ns††	20–200 ns‡‡
Micro-pattern gas detector	30–40 μm	5–10 ns††	20–200 ns‡‡
Silicon strips/pixels	$\lesssim$ 10 μm§§	few ns¶¶ ‡‡	$\lesssim$ 50 ns‡‡

- 40 MHZ bunch crossing rate
- Good spatial resolution needed for measuring pT

Efficiency:

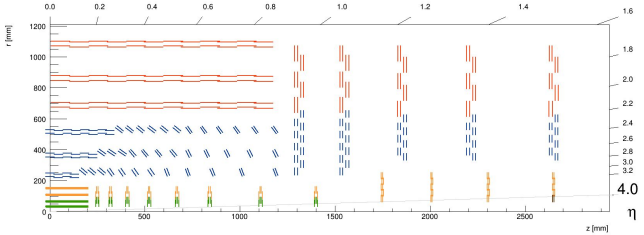
Goal: 99% efficiency for min ionizing start of lifetime

Radiation Hardness:

1.3 Radiation requirements

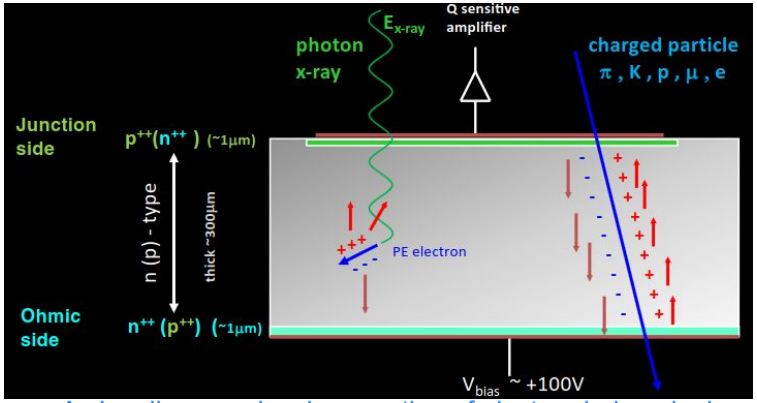
The increase of LHC luminosity also results in significantly increased radiation levels in the pixel detector. For 10 years operation the inner pixel layers should ideally remain functional after ˜1.4Grad (even up to 1.9Grad in the ultimate running scenario of CMS). This has been

Layers:

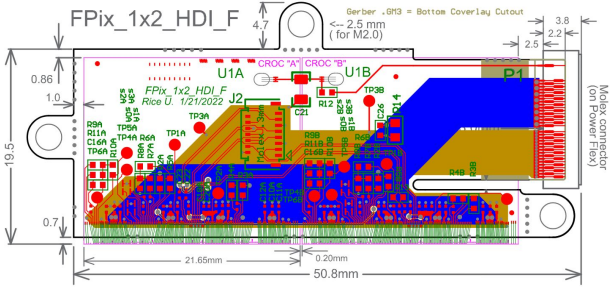


RD53B

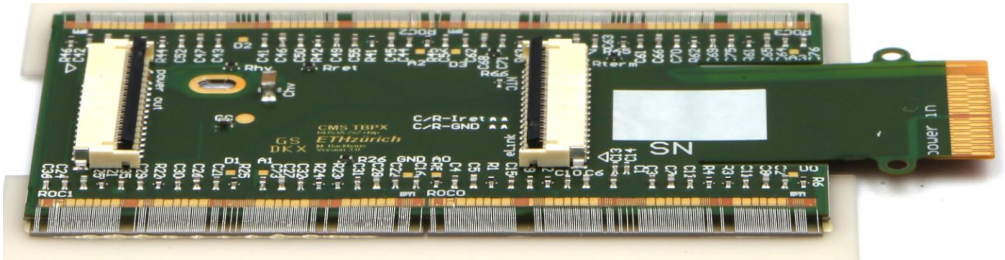
- RD53 designed two modular pixelated silicon sensors
- 2x1(2 chips, ~300k pixels) and 2x2 (4 chips ~600k pixels)
- ~ 2 billion total readout channels
- Fairly radiation hard, but at end of life, e-h pairs can be created thermally reducing efficiency



A nice diagram showing creation of electron hole pairs in silicon, taken from this presentation by Cinzia Da Via



The floorplan of a 2x1 module



A real 2x2 module, from the side, stolen from Malte Backhaus here

What are we doing?

Design of modules completed by RD53 collaboration

Chips manufactured by Taiwan Semiconductors

Bump bonding silicon to readout chip (CROC) Micross?

Assemble chips with high density interconnect (HDI), wirebonding

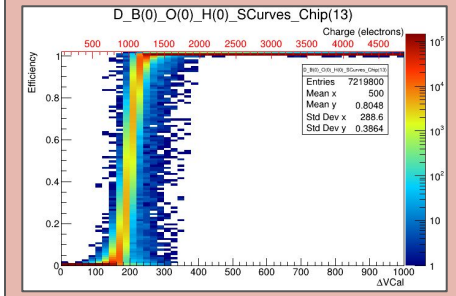
Perform QC testing

Perform electronics testing

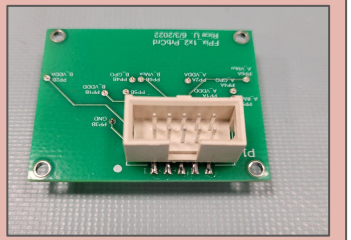
Perform thermal testing
Assemble to dee and test on dee

What are we doing?

Individual module electronic testing



S curves: A turn-on curve

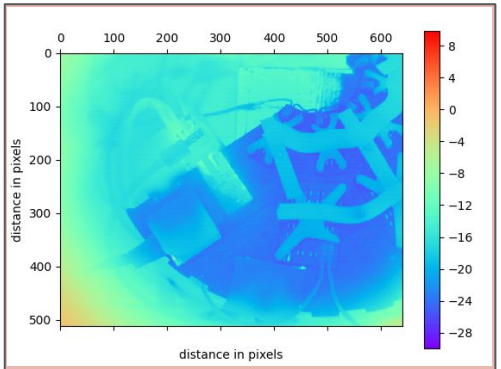


Probe card to test module powering

Assembly on dee

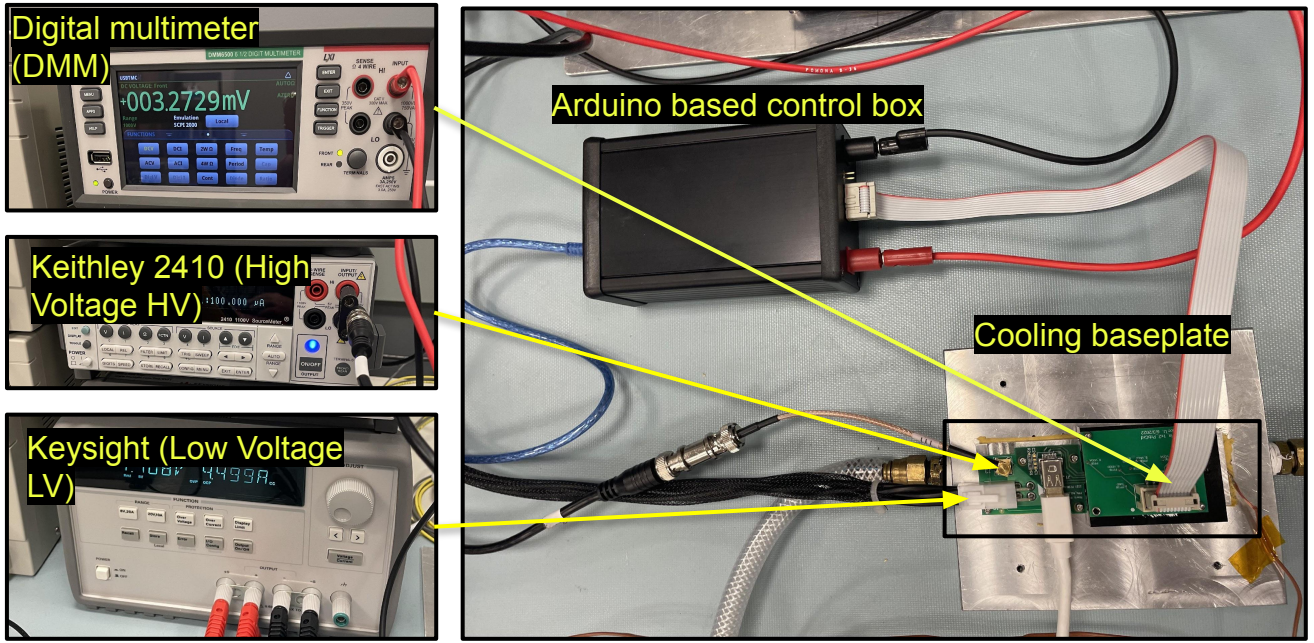
Thermal testing

See other talks today :)



Thermal image of module on dee

Hardware Interface



Software+Firmware Interface

CMS Phase 2 Acquisition and Control Framework (Ph2_ACF)

Available scans/calibrations are:

1. Latency scan ➜ `latency`
2. PixelAlive ➜ `pixelalive`
3. Noise scan ➜ `noise`
4. SCurve scan ➜ `scurve`
5. Gain scan ➜ `gain`
6. Threshold equalization ➜ `threqu`
7. Gain optimization ➜ `gainopt`
8. Threshold minimization ➜ `thrmin`
9. Threshold adjustment ➜ `thradj`
10. Injection delay scan ➜ `injdelay`
11. Clock delay scan ➜ `clkdelay`
12. Bit Error Rate test ➜ `bertest`
13. Data read back optimisation ➜ `datarbopt`
14. Chip internal voltage tuning ➜ `voltagetuning`
15. Generic DAC-DAC scan ➜ `gendacdac`
16. Physics ➜ `physics` / `eudaq`, used for data talking (e.g. in testbeams)

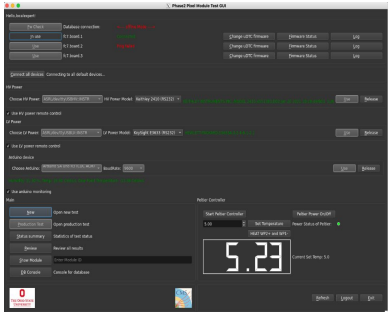
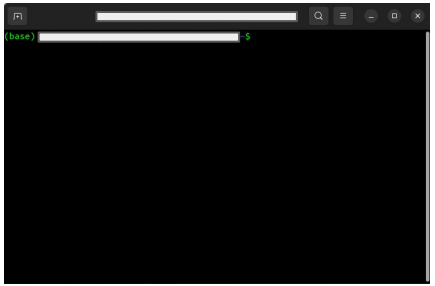


Image of OSU Gui from Matt Joyce

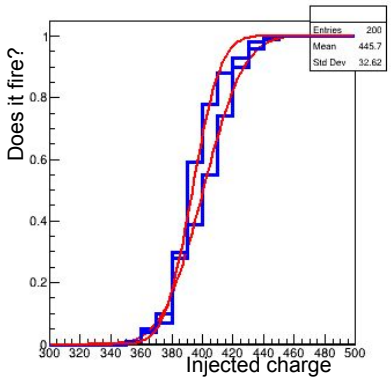


Can also test from terminal!

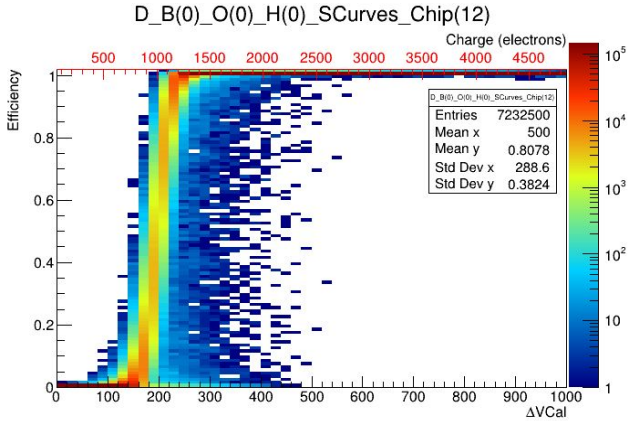
FC7 FPGA board

How to read an S-Curve

- S-Curve represents pixel turnon: 0 means pixel not responding, 1 means sends out expected pulse
- Measure as a function of injected charge (simulate a particle hit)



×140000

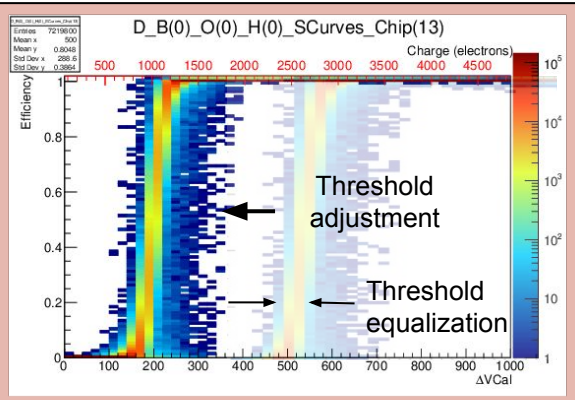


Inject charge into pixel, measure if it fires

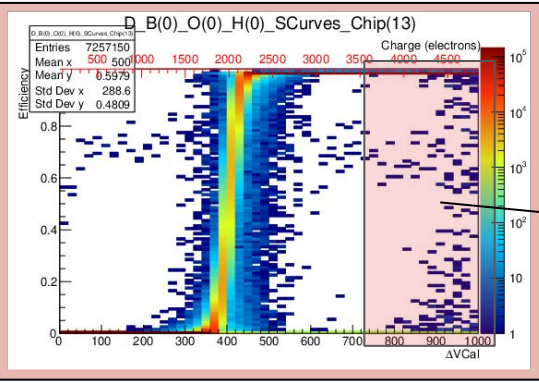
Repeat for every pixel on module

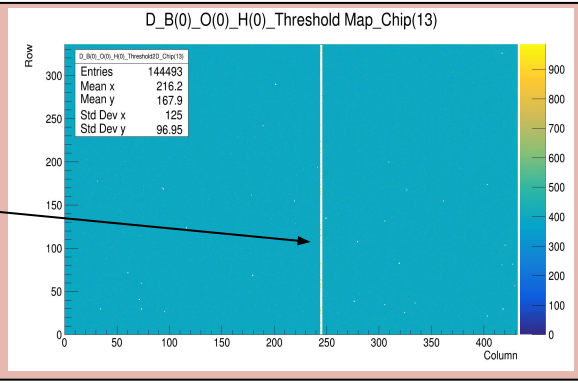
Trimming procedure

- Reduce turn on point (higher efficiency!)
- Perform in steps:
  - Lower threshold (turn on point) “thradj”
  - Make all pixels behave identically “threqu”
  - View S curve “scurve”
  - Mask noisy pixels
  - Repeat from start

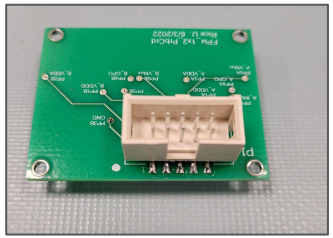


Also be on look out for odd behavior
(should just be clean sigmoid)

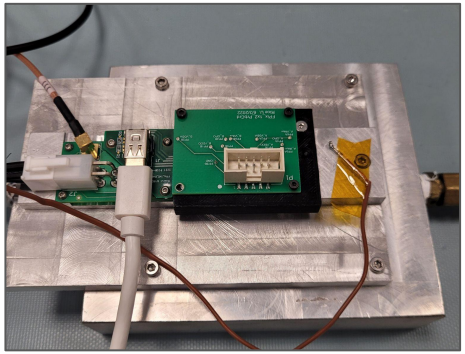




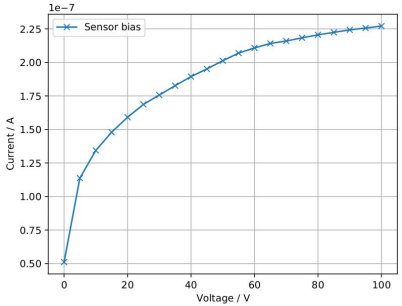
Probe needle measurements



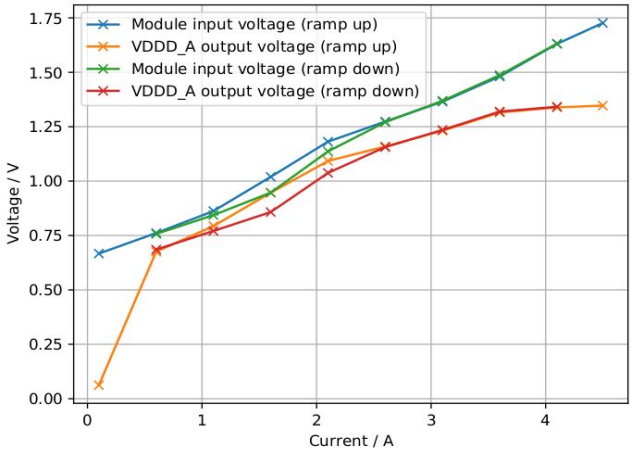
Probe card tests for anomalies in module powering



Test IV behavior: should be diode like



Example SLDO Curve



Modules have multiple chips being powered by same power source, but must not receive extra power if one of the chips breaks
-SLDO powers each chip up to 1.25 V, but not higher.

The Future

Prototype module testing continues

- Receiving new modules soon
- Module testing workshop late Feb

Serial module powering

- Needs to be tested in order to run a real dee!

Big hurdles to overcome!

Coldboxes, cleanrooms, new hardware, much to do

Minimal module testing prior to assembly

- Important portion of assembly process

Thermal and electronic testing of multiple modules on dee

- Confirm thermal performance of dee with real modules
- Ensure modules not damaged during assembly to dee